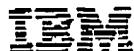


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(A) AMENDMENT OF THE CLAIMS:

1 1. (Currently Amended) An integrated circuit, comprising  
2 logic circuits connected to a plurality of shift register  
3 latch scan chains and self-test circuits for testing said  
4 logic circuits, said self-test circuits in said integrated  
5 circuit comprising:

6 a pseudo-random pattern generator for generating at  
7 least one flat pseudo-random patterns to provide to each of  
8 the scan chains;

9 A plurality of weighting circuits for receipt of the  
10 pseudo-random patterns from the pattern generator, a  
11 different one of the weighting circuits associated with each  
12 of the scan chains, each weighting circuit having a  
13 selectable weight set to provide flat or weighted pseudo-  
14 random patterns to the scan chains independently of one  
15 another;

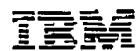
16 a different storage element associated with each of the  
17 weighting circuits for receipt and storage of flat and  
18 weighted pseudo-random patterns each from its different  
19 associated weighting circuit; and

20 a selection circuit for individually addressing each of  
21 the storage elements selective entry of either a flat or  
22 weighted pseudo-random pattern into different shift register  
23 latches of said scan chains independently of one another for  
24 scanning said weighted pattern to said logic circuits to  
25 enable provision of pseudo-random patterns of different  
26 weights to different shift register latches in the same scan  
27 chain.

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1 2. (Original) An integrated circuit as recited in claim 1,  
2 wherein said weighting circuit comprises a weight generating  
3 circuit and a weight selecting circuit.

1 3. (Original) The integrated circuit as recited in claim  
2 1, wherein said weighting circuit includes means for  
3 receiving a weighting instruction from an external source to  
4 said integrated circuit.

1 4. (Original) The integrated circuit as recited in claim  
2 1, wherein said storage elements are each a first stage of  
3 an associated scan chain.

1 5. (Currently Amended) The integrated circuit as recited  
2 in claim 4, wherein said pseudo-random pattern generator  
3 and said weighting patterns, receipts pattern and weighting  
4 instructions are from a tester internal to said integrated  
5 circuit.

1 6. The integrated circuit as recited in claim 4, wherein  
2 said weighting instruction is generated by a tester external  
3 to said integrated circuit.

1 7. (Original) The integrated circuit as recited in claim  
2 4, further comprising a memory or register array wherein at  
3 least a portion of said weighting instruction is stored in  
4 said memory array.

1 8. (Cancelled)

1 9. (Cancelled)

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1 10. (Currently Amended) The integrated circuit of claim 1,  
2 wherein said pseudo-random pattern generator is a linear  
3 feedback shift register coupled to each of the weighting  
4 circuits to provide a flat pseudo-random pattern to each of  
5 the weighting circuits.

1 11. (Previously submitted) The integrated circuit of claim  
2 10, wherein the scan paths contain multiple shift register  
3 latch stages SRL<sub>1</sub> to SRL<sub>n</sub> each with first and second stages  
4 which SRL stages are controlled by an A clock, a B clock and  
5 a C<sub>1</sub> clock.

1 12. (Previously submitted) The integrated circuit of claim  
2 11, wherein the first shift register stage SRL of each scan  
3 chain functions as said storage element associated with the  
4 scan chain and received at its L<sub>1</sub> latch an input from the  
5 associated weighting circuit, an address input from an  
6 address decoder of the selection circuit and a w-clock for  
7 separately addressing each of the scan paths to enable entry  
8 of data from an associated weighting circuit into the first  
9 stage of the scan path on a SRL by SRL of the scan path  
10 basis.

1 13. (Previously submitted) The integrated circuit of claim  
2 12 including means performing the following loading sequence  
3 steps individually for each of the plurality of scan paths:  
4 generating the next flat or weighted pseudo-random  
5 pattern;  
6 applying the L<sub>1</sub> scan clock (A-clk\_) to load all the L<sub>1</sub>  
7 Latches of the register array with flat or weight  
8 pseudo-random data from the LFSR;

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9        updating an L1 in any specific SRL1 stage scan path by  
10    addressing the particular L1 latch stage and applying the  
11    w-clock;  
12        loading the L2 latch from the L1 latch (B-clk); and  
13        repeating all the steps until the longest scan chain is  
14    loaded.